Project description Oberseminar 2017

Topic: SDN hardware acceleration

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SDN is one of today key technologies in modern networks. SDN enables an software based network definition by one or multiple control entities. The disadvantage of software based packet processing is the introduced delay in comparison to pure hardware solutions. Therefore hybrid devices with SDN acceleration units are used to provide the full feature-set of SDN(e.g. OpenFlow) in software and accelerate some rules in hardware. Of course the hardware acceleration units can't have the same features and table-sizes like the software implementation of SDN switches. The question is, how to map the SDN rules from software to hardware, by not breaking the rules dependencies? Kaplayan [1][1] gives an detailed view on a SDN acceleration implementation. Your task is to do a source research for existing mapping rules and techniques to transfer rules from an full SDN switch(e.g. OVS) to an hardware acceleration structure with a restricted feature set. (e.g. Flowcache @ TrustNode [2])
Todo:

- do research
- collect all suitable solutions
- compare them
- write a report(with LaTeX) using the collected content
- prepare a presentation

References

[1] G. Kaplayan, "Software-defined network packet classification on FPGA," Master's thesis, Technical University Munich, 2017.

[2] C. Liß, M. Ulbricht, U. F. Zia, *et al.*, "Architecture of a synchronized Low-Latency network node targeted to research and education," in *2017 IEEE 18th International Conference on High Performance Switching and Routing (HPSR) (IEEE HPSR'17)*, Campinas, Brazil, Jun. 2017. [Online]. Available: `https://innoroute.com/wp-content/uploads/2017/06/HPSR17-TN.pdf`.

[1] Download the document here.