Investigation of Intel Time-coordinated Computing for TSN

Project topic adaptable for Oberseminar, Student Thesis, Bachelor, or Master/Diploma-Thesis

Reference: nist.gov

Objective of Work

Time-sensitive applications are characterized by stringent timing requirements, where even minor deviations such as jitter or latency exceeding a specified threshold can degrade communication quality. Such applications are increasingly emerging in domains such as the Tactile Internet and industrial automation. To address these challenges, Time-Sensitive Networking (TSN) provides deterministic communication through preplanned and time-triggered packet transmissions.

In these systems, precise packet generation and transmission are essential to ensure deterministic performance. Typically, packets are generated as periodic streams within repetitive cycles; however, host systems executing these applications often exhibit timing jitter, preventing the generation cycle from occurring with exact regularity. This temporal inaccuracy results in missed deadlines, loss of allocated transmission windows, or unintended queuing effects.

Time-Coordinated Computing (TCC), introduced by Intel, represents a set of architectural features integrated into various Intel CPU families to enhance timing determinism across the computing and communication layers. TCC enables synchronization between application-level processes and the underlying hardware, ensuring that packets are prepared and released precisely at the intended transmission times. It comprises mechanisms for cache allocation, core frequency boosting, and core isolation, collectively designed to prioritize real-time workloads and minimize

interference from non-deterministic system activities. Despite these developments, a lack of systematic evaluation remains regarding TCC's influence on **timely packet generation** and its practical contribution to deterministic communication. The objective of this work is to analyze and quantify the impact of TCC features on the temporal precision of real-time packet generation and transmission.

Focus of Work

In the thesis, the following tasks should be addressed:

- Literature review & conceptual Analysis
- System setup: build a synchronized sender–receiver testbed with a TCC-enabled sender executing cyclic real-time loops.
- Intel TCC optimization: following the Intel guidelines, tune the real-time application and system to reduce latency and jitter.
- Compare performance with and without TCC features across different cycle periods to quantify the improvements in jitter and latency.
- (Optional) TSN scheduling integration: design TSN schedules aligned with TCC-enhanced compute timing for coordinated end-to-end determinism.
- Documentation and presentation of the work and results in a scientific way.

Material for Further Reading

- Characterization of latency and jitter in TSN emulation
- TCC guidelines
- Time Coordinated Computing mode

Keywords

Intel TCC, Time-Synchronization, End-to-End configuration, Optimization

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